IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: GARY M. JOHNSON	Group Art Unit: 2816
Serial No.: 10/733,605	Examiner: Dinh Thanh Le
Filed: DECEMBER 11, 2003	Conf. No.: 8519
	Atty. Dkt.: 2008.007900/03-0478
For: SWITCHED CAPACITOR FOR A TUNABLE DELAY CIRCUIT	CUSTOMER NO.: 23720

APPEAL BRIEF

MAIL STOP APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

On May 8, 2007, Appellant filed a Notice of Appeal in response to a Final Office Action dated January 8, 2007 issued in connection with the above-identified application. In support of the appeal, Appellant hereby submits this Appeal Brief to the Board of Patent Appeals and Interferences.

Since the Notice of Appeal for the present invention was received and stamped by the USPTO Mailroom on May 14, 2007, the two-month date for filing this Appeal Brief is July 14, 2007. This Appeal Brief is being electronically filed on July 16, 2007 (since July 14, 2007 falls on a Saturday), therefore, it is timely filed.

If an extension of time is required to enable this paper to be timely filed and there is no separate Petition for Extension of Time filed herewith, this paper is to be construed as also

constituting a Petition for Extension of Time Under 37 CFR § 1.136(a) for a period of time sufficient to enable this document to be timely filed.

The Commissioner is authorized to deduct the fee for filing this Appeal Brief in the amount of $500.00 from Williams, Morgan & Amerson, P.C.'s PTO Deposit Account No. 50-0786/2008.007900. No other fee is believed to be due in connection with the filing of this document. However, should any fee under 37 C.F.R. §§ 1.16 to 1.21 be deemed necessary for any reason relating to this document, the Commissioner is hereby authorized to deduct said fee Williams, Morgan & Amerson, P.C.'s PTO Deposit Account No. 50-0786/2008.007900

I. REAL PARTY IN INTEREST

The present application is owned by Micron Technology, Inc.

II. RELATED APPEALS AND INTERFERENCES

Appellant is not aware of any related appeals and/or interferences that might affect the outcome of this proceeding.

III. STATUS OF CLAIMS

Claims 1-10 and 25-44 remain pending in this application and are the subject of this appeal.

Claims 5-8, 29-32 and 39-42 are objected to under 35 U.S.C. 112, 2nd paragraph, but would be allowable if rewritten to include all limitations of the base claim.

Claims 1-4, 9, 10, 35-38 and 43-44 are rejected under 35 U.S.C. §103(a) as being unpatentable over ***Lee*** (U.S. Patent No. 6,483,359) in view of ***Johnson*** (U.S. Patent No. 5,101,117).

Claims 1-4, 9-10, 25-28, 33-38 and 43-44 are rejected under 35 U.S.C. §103(a) as being unpatentable over ***Baker*** in view of ***Lee*** and further in view of ***Johnson***.

IV. STATUS OF AMENDMENTS

After the Final Rejections, no other amendments were made to any other claims.

V. SUMMARY OF CLAIMED SUBJECT MATTER

In one aspect of the instant invention, a device is provided to perform switching of capacitance in a delay lock loop, as called for by claim 1 of the present invention. The device of the present invention includes a delay lock loop (230) to provide an output signal based upon a phase difference between a reference signal and a feedback signal. The delay lock loop (230) includes a delay circuit (410) for switching an activation of a transistive capacitive delay. *See Specification, page 5, lines 1-6; page 11, line 1-page 13, line 2; page 15, lines 1-17; page 16; lines 18-page 19, line 15; Figures 2, 4, 5.*

In yet another aspect of the instant invention, a system board is provided to perform switching of capacitance in a delay lock loop (230), as called for by claim 25 of the present invention. The system board of the present invention includes a first device (110). The first device (110) includes a memory location for storing data and a delay lock loop (230) to provide an output signal based upon a phase difference between a reference signal and a feedback signal. The delay lock loop (230) includes a delay circuit (410) for activating a transistive capacitive delay. The delay lock loop (230) also includes a second device (125) operatively coupled to the first device (110). The second device (125) to access the data from the first device (110) based upon an operation performed by the delay lock loop (230). *See Specification, page 6, lines 4-9;*

page line12-page 10, line 24; page 15, lines 1-17; page 16; lines 18-page 19, line 15; Figures 1, 4, 5.

In one aspect of the instant invention, a memory device (130) is provided to perform switching of capacitance in a delay lock loop, as called for by claim 1 of the present invention. The device of the present invention includes a delay lock loop (230) to provide an output signal based upon a phase difference between a reference signal and a feedback signal. The delay lock loop (230) includes a delay circuit (410) for switching an activation of a transistive capacitive delay. *See Specification, page 5, lines 1-6; page 11, line 1-page 13, line 2; page 15, lines 1-17; page 16; lines 18-page 19, line 15; Figures 2, 4, 5.*

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Whether claims 1-4, 9-10, 35-38 and 43-44 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,483,359 (***Lee***) in view of U.S. Patent No. 5,101,117 (***Johnson***);

2. Whether claims 1-4, 9-10, 25-28, 33-38 and 43-44 stand rejected under 35 U.S.C. §103(a) as being unpatentable over ***Baker*** in view of ***Lee*** and further in view of ***Johnson***; and

3. Whether claims 5-8, 29-32 and 39-41, which as admitted by the Examiner contains allowable subject matter, are allowable.

VII. ARGUMENT

The present invention is directed to implementing a delay, such as a fine tuned delay in a delay lock loop circuitry to provide more synchronized transmission of signals in and/or out of an electronic device, such as a memory device. The present invention teaches implementing

capacitive delays in a fine delay environment in a delay lock loop circuit. Claims of the present invention are directed to a delay lock loop that is capable of providing an output signal based upon a phase difference between a reference signal and a feedback signal. The delay lock loop includes a delay circuit for activating a transistive capacitive delay. The Examiner relies heavily upon U.S. Patent No. 6,483,359 (***Lee***) and U.S. Patent No. 5,101,117 (***Johnson***) to reject the claims. However, none of the cited prior art, alone or in combination, anticipate or make obvious any of the pending claims of the present patent application. ***Lee*** is directed to a passive capacitor that may be connected to the inverted clock signal, and does not disclose a transistive capacitive delay for use in a delay circuit of a delay lock loop. ***Johnson*** does not make up for the lack of disclosure of ***Lee***. ***Johnson*** is directed to passive capacitors. Neither of these prior art references suggest using a transistive capacitive delay for a delay circuit in a delay lock loop. Contrary to Examiner's assertion the combination of ***Lee*** and ***Johnson*** do not make obvious all of the elements of claims of the present invention. Other cited prior art also do not make up for the deficit of ***Lee*** and ***Johnson***. The Examiner cited U.S. Patent No. 6,445,231 (***Baker***) to combine it with ***Lee*** and ***Johnson*** to reject claims of the present application. However, ***Baker*** clearly does not disclose the delay circuit at all, much less a delay circuit for activating a transistive capacitor delay. Hence, the cited prior art references, alone or in combination, do not make obvious all of the elements of claims of the present invention. Accordingly, the Examiner erred in maintaining the rejections of claims of the present invention.

The specific claims of the present invention are discussed below.

A. **Claims 1-4, 9-10, 35-38 And 43-44 Are Not Unpatentable under 35 U.S.C. § 103(a) under U.S. Patent No. 35 U.S.C. §103(a) Under U.S. Patent No. 6,483,359 (*Lee*) in view of U.S. Patent No. 5,101,117 (*Johnson*)**

The Examiner rejected claims 1-4, 9-10, 35-38 and 43-44 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,483,359 (***Lee***) in view of U.S. Patent No. 5,101,117 (***Johnson***). Appellant respectfully asserts that the Examiner erred in maintaining this rejection.

Appellant respectfully asserts that the combination of ***Lee*** and ***Johnson*** do not teach, disclose, or make obvious all of the elements of claims of the present invention. In the Final Office Action dated January 8, 2007, the Examiner addresses one of Appellant's various arguments provided in the previous Response to Office Action. In the Final Office Action, the Examiner asserted that ***Lee*** allegedly discloses transistive capacitive delay and asserts that the capacitance of delay circuits are activated by transition of gate voltages applied to gate switches. However, as described in greater detail below, ***Lee*** simply does not disclose transistive capacitances, as called for by claims of the present invention. Under the Examiner's theory, even a light bulb that is switched by a gate switch would become an active transistive device, which is simply incorrect reasoning. Simply because passive capacitive may or may not be activated by a different set of switches, does not make them transistive capacitances. This is described in greater detail below. Further, as described below, ***Johnson***, does not make up for this deficit for various reasons. In the Final Office Action, the Examiner did not address these arguments and simply reasserted that ***Johnson*** comprises transistive capacitors. ***Johnson*** simply discloses passive capacitors (*72a-l*). Simply because capacitances are disclosed in an alternative prior art reference does not mean those skilled in the art would apply it the way it is called for by claims of the present invention. The Examiner provides no real connection between the prior art references, and as further described below, without using improper hindsight reasoning, ***Johnson***

and ***Lee*** would not be combined to make obvious all of the elements of the claims of the present invention.

Contrary to the Examiner's assertions in the Final Office Action, Appellant respectfully asserts that the combination of ***Lee*** and ***Johnson*** does not teach, disclose, or make obvious all of the elements of claim 1 of the present invention. Appellant respectfully asserts that all of the elements of independent claims 1 and 35 are not taught, disclosed, or suggested by ***Lee***. The Examiner merely listed a few elements, such as a phase detector, a first delay line and a second delay line and a feedback line of ***Lee*** to assert anticipation of claims 1 and 35. The Examiner merely provides conclusory statements, equating the delay lines of ***Lee*** to the course delay circuit and the fine delay called for by claims of the present invention. In other words, the Examiner merely lists various reference numbers next to certain words out of the elements of claims of the present invention. ***Johnson*** does not make up for this deficit. Appellant respectfully asserts that ***Lee*** and ***Johnson*** does not teach, disclose, or suggest all of the elements of claims 1 and 35 of the present invention.

The Examiner uses the capacitors (capacitor 60 of Figure 3 and capacitors 72a-72l of Figure 4) of ***Johnson*** and the capacitors C1, C2, C3, in Figures 4, and 6A through 6D of ***Lee*** to argue anticipation of elements of the claims of the present invention. However, Appellant respectfully asserts that claims 1 and 35 of the present invention call for a delay lock loop that comprises a delay circuit for activating a transistive capacitive delay. In contrast, the disclosure of ***Lee*** merely refers to a passive capacitor that may be connected to the inverted clock signal, as described in Figures 4 and 6A-6D of ***Lee***. Further, ***Johnson*** doesn't make up for this deficit. The Examiner provides no explanation or arguments as to how the disclosure of ***Lee*** anticipates elements of claims of the present invention. Further, ***Lee*** simply does not disclose a transistive

capacitive delay, as called for by claims 1 and 35 of the present invention. Various advantages of implementing the present invention are achieved over the prior art. For example, the Specification discloses the issue of an RC time constant that may become problematic when applying the standard passive capacitor, as disclosed by ***Lee***. Further, utilizing the transistive capacitive elements, an advantage of providing for a relatively constant capacitance during voltage transitions may be achieved, which is a feature that is not provided by ***Lee***. *See* Specification, p.19, lines 3-15. Therefore, various exemplary advantages may be achieved utilizing the transistive capacitive disclosed by claims 1 and 35. Therefore, different problems are addressed by the present invention, in comparison to the problems addressed by the prior art. ***Lee*** simply does not disclose activating a transistive capacitive delay, as called for claims 1 and 35 of the present invention. Therefore, ***Lee*** clearly does not anticipate all of the elements of claims 1 and 35 of the present invention.

The Examiner attempts to make up for the deficit of ***Lee*** by adding the disclosure of ***Johnson*** to make obvious the transistor capacitor delay. Aside from being non-analogous art, ***Johnson*** does not make up for the deficits of ***Lee***.

In the Final Office Action, the Examiner asserted that ***Johnson*** and ***Lee*** would be combined by those skilled in the art because they both relate to delay circuit. However, this is an overbroad assessment, under which one could use improper hindsight reasoning to combine practically any prior art reference to tailor arguments for obviousness. Clearly, this is improper. ***Johnson*** is merely directed to a system for synchronizing the operation of a CPU and a co-processor. ***Johnson*** discloses a FPC chip 20 capable of accessing system data-bus in order to synchronize the data access. *See* column 3, lines 1-5. ***Johnson*** discloses a phase detector that supplies an output indicative of the phase difference of the signals received on line 18, which is a

CPU output enable signal and on line 19, which is an FPC output enable signal. *See* column 3, lines 5-8. Therefore, the phase detector of ***Johnson*** is not directed towards data transfer, it is directed towards enabling two different entities. ***Johnson*** does not disclose a feedback signal for using the phase detector. Therefore, ***Johnson*** is entirely different and non-analogous to ***Lee*** and those skilled in the art would not be motivated to combine them to make obvious all of the elements of claims of the present invention.

The present invention calls for detecting the phase difference between a reference signal and a feedback signal and then using a delay circuit for activating a transistive capacitive delay. These are elements that are not disclosed or suggested by either ***Lee*** or ***Johnson***, or a combination of the two. ***Johnson*** does not disclose or make obvious transistive capacitances. The Examiner incorrectly identifies the capacitors 72a-72l in Figure 4 as a transistive capacitor. The Examiner is false in this assertion. The capacitors shown in Figure 4 (72a-72l) are actually simple **passive** capacitors whose connection is influenced by the transistors 71a-71l. *See* Figure 4 of ***Johnson***. ***Johnson*** clearly discloses that the delay line in Figure 4 consists of a series of drivers and control transistors 71a-71l and 12 capacitors 72a-72l. *See,* column 4, lines 39-44. Therefore, neither ***Lee*** nor ***Johnson*** discloses or makes obvious a transistive capacitor. Similarly, the Examiner's citation of the capacitor 60 in Figure 3 of ***Johnson*** is also similarly false since the capacitor 60 is simply a passive capacitor. Contrary to the Examiner's position, in the Final Office Action, simply because a passive capacitor is switched by a switch doesn't make it a transistive capacitance. This is clearly improper hindsight tailoring of arguments based upon prior art. In the Final Office Action, the Examiner merely asserts that the capacitors in ***Johnson*** are transistive, without providing reasoning. Accordingly, ***Johnson*** also has all of the

weaknesses of ***Lee*** and the combination of ***Johnson*** and ***Lee*** do not teach, disclose or suggest all of the elements of the claims of the present invention.

To establish a *prima facie* case of obviousness, three basic criteria must be considered. Firstly, the factor of the prior art reference (or references when combined) teaching or suggesting all the claim limitations must be analyzed. As described above, the combination of ***Lee*** and ***Johnson*** do not teach or suggest all of the elements of claims 1 and 35 of the present invention.

Secondly, the factor relating to the some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings, should also be considered. Appellant respectfully asserts that the Examiner has provided no evidence, nor is there any evidence in the cited prior art that would provide an indication of motivation of those skilled in the art to combine ***Lee*** and ***Johnson*** to read upon all of the elements of claims 1 and 35 of the present invention. Contrary to the Examiner's contention, those skilled in the art simply would not find motivation to combine ***Johnson*** and ***Lee***.

The Examiner asserted that those skilled in the art would allegedly combine ***Johnson*** and ***Lee*** for the purpose of reducing size by employing the transistive capacitor. There are at least two flaws in this reasoning. First, neither ***Johnson*** nor ***Lee*** discloses transistive capacitors. Secondly, reduction of size is not a motivation to use the transistive capacitor, there are other motivations (which are not present in any of the cited prior art) exemplified above, such as the advantage of providing a relatively constant capacitance during voltage transitions. These are motivations that are not addressed or anticipated by ***Lee*** nor ***Johnson***. Without improper hindsight, those skilled in the art simply would not find the motivation to combine the delay lock loop of ***Lee*** with the data path disclosure of ***Johnson*** to make obvious all of the elements of

claims 1 and 35. Therefore, there is no evidence or motivation, either in the references themselves or in the knowledge, generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings.

Third, the factor relating to a reasonable expectation of success by combining the prior art, should also be considered. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Appellant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991); M.P.E.P. § 2142. There is no evidence that the improbable combination of ***Lee*** and ***Johnson*** provide a reasonable expectation of success. There is no evidence to a contrary assertion, and the Examiner fails to provide any evidence of reasonable expectation of success based upon the prior art. Therefore, the Examiner failed to establish a *prima facie* evidence of obviousness with respect to claims 1 and 35 of the present invention. Accordingly, for a least the reasons described above ***Lee*** and ***Johnson*** do not cause all of the elements of claims 1 and 35 to be are taught, disclosed, or suggested. The Examiner failed to show a *prima facie* case of obviousness of claims 1 and 35. Accordingly, independent claims 1 and 35 are allowable. Further, dependent claims 1-4, 9-10 which depend from claims 1, and claims 36-38, 43-44, which depend from claim 35, are also allowable for at least the reasons cited herein.

B. Claims 1-4, 9-10, 35-38 And 43-44 Are Not Unpatentable under 35 U.S.C. § 103(a) under U.S. Patent No. 35 U.S.C. §103(a) Under U.S. Patent No. 6,445,231 (Baker) In View Of U.S. Patent No. 6,483,359 (*Lee*) And In Further View of U.S. Patent No. 5,101,117 (*Johnson*)

Claims 1-4, 9-10, 25-28, 33-38 and 43-44 remain rejected under 35 USC 103(a) as being unpatentable over U.S. Patent No. 6,445,231 (***Baker***) in view of U.S. Patent No. 6,483,359

(***Lee***) and further in view of U.S. Patent No. 5,101,117 (***Johnson***). Appellant respectfully asserts that the Examiner erred in maintaining this rejection.

Contrary to the Examiner's assertion in the Final Office Action, as described above, ***Lee*** clearly does not disclose many of the elements of claim 1 of the present invention. The inclusion of ***Johnson*** and ***Baker*** does not make up for this deficit. The Examiner stated that ***Baker*** does not disclose the DLL circuit comprising delay circuit as recited in claims 1, 25 (as amended), and 35. The Examiner then uses ***Lee*** and ***Johnson*** to make up for this deficit. However, ***Baker*** clearly does not disclose the delay circuit at all, much less a delay circuit for activating a transistive capacitor delay. As described above, neither ***Lee*** nor ***Johnson*** discloses a delay circuit for activating a transitive capacitor delay. Therefore, the combination of ***Baker***, ***Lee*** and ***Johnson***, does not teach, disclose, or suggest all of the elements of claim 1 of the present invention. Hence, the first prong of showing a *prima facie* obviousness is not shown.

Further, those skilled in the art would not combine ***Baker*** with ***Lee*** and/or ***Johnson*** to make obvious all of the elements of claim 1 of the present invention. Simply because ***Lee*** and ***Johnson*** disclose a DLL loop, the Examiner failed to provide any evidence motivation why those skilled in the art would combine them to make obvious the elements of claim 1, 25, and 35 of the present invention, particularly, the delay circuit for activating a transistive capacitive delay. Nothing in ***Lee*** discloses or suggests that those skilled in the art would look for a solution for the transistive capacitor delay and attempt to combine any prior art cited. Hence, the second prong of showing a *prima facie* obviousness is not shown.

Additionally, there is no evidence that the improbable combination of ***Baker***, ***Lee*** and ***Johnson*** provide a reasonable expectation of success. There is no evidence to a contrary

assertion, and the Examiner fails to provide any evidence of reasonable expectation of success based upon the prior art. Hence, the third prong of showing a *prima facie* obviousness is not shown. However, as described above, even if all of the cited prior art were combined, all of the elements of claims 1, 25, and 35 of the present invention would not be taught, disclosed or suggested. As described above, the Examiner failed to provide a *prima facie* showing of obviousness of claims 1, 25, and 35. Therefore, independent claims 1, 25, and 35 of the present invention are allowable for at least the reasons cited herein. Further, dependent claims 1-4, 9-10, which depend from claim 1; claims 26-28, 33-34, which depend from claim 25; and claims 36-38, 43-44, which depend from claim 35 are also allowable for at least the reasons cited herein.

C. Claims 5-8, 29-32, and 39-41 Contain Patentable Subject Matter, As Indicated By The Examiner, And Are Allowable.

Appellant acknowledges that the Examiner has indicated that claims 5-8, 29-32 and 39-41 contain allowable subject matter; however, in light of the arguments presented herein, all pending claims of the present invention are allowable. These claims depend from allowable claims, as described above. Therefore, the Examiner erred in maintaining the rejection of claims 5-8, 29-32 and 39-41 under 35 U.S.C. 112, 2nd paragraph. Therefore, claims 5-8, 29-32 and 39-41 are allowable. Therefore, Appellant respectfully solicits a Notice of Allowance, allowing claims 1-10 and 25-44 of the present invention.

VIII. CLAIMS APPENDIX

The claims currently under consideration, *i.e.,* claims 1-10 and 25-44 are listed in the Claims Appendix attached hereto.

IX. EVIDENCE APPENDIX

There is no evidence relied upon in this Appeal with respect to this section.

X. RELATED PROCEEDINGS APPENDIX

There are no related appeals and/or interferences that might affect the outcome of this proceeding.

In view of the foregoing, it is respectfully submitted that the Examiner erred in not allowing all claims (claims 1-10 and 25-44) pending in the present application over the prior art of record. The undersigned attorney may be contacted at (713) 934-4069 with respect to any questions, comments, or suggestions relating to this appeal.

Respectfully submitted,
WILLIAMS, MORGAN & AMERSON, P.C.

Date: July 16, 2007

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CLAIMS APPENDIX

1. (Previously Presented) A device, comprising:

delay lock loop to provide an output signal based upon a phase difference between a reference signal and a feedback signal, said delay lock loop comprising a delay circuit for activating a transistive capacitive delay.

2. (Original) The device of claim 1, wherein said device is a memory device.

3. (Original) The device of claim 2, wherein said memory device is at least one of a static random access memory (SRAM), a dynamic random access memory (DRAM), a double-data rate SDRAM (DDR SDRAM), a DDR I device, a DDR II device, a Rambus DRAM (RDRAM), and a FLASH memory.

4. (Previously Presented) The device of claim 1, wherein said delay lock loop further comprises:

a coarse delay unit to provide a coarse delay upon at least one of said reference signal and a data output signal;

a fine delay unit to provide a fine delay upon at least one of said reference signal and said data output signal;

a phase detector to detect said phase difference; and

a feedback delay unit operatively coupled to said coarse delay unit, said fine delay unit, and said phase detector, said feedback delay unit to provide a delay upon said output signal to generate said feedback signal.

5. (Previously Presented) The device of claim 4, wherein said fine delay unit comprises:

a first inverter to invert an input signal;

an N-channel transistor set operatively coupled to said first inverter, said N-channel transistor set comprising a first and a second N-channel transistor, wherein a source terminal of said first N-channel transistor is coupled to a source terminal of said second N-channel transistor and a drain terminal of said first N-channel transistor is coupled to a drain terminal of said second N-channel transistor;

an P-channel transistor set comprising a first and a second P-channel transistor, wherein a source terminal of said first P-channel transistor is coupled to a source terminal of said second P-channel transistor and a drain terminal of said first P-channel transistor is coupled to a drain terminal of said second P-channel transistor; and

a second inverter operatively coupled to said P-channel transistor, said second inverter to provide a complementary control signal for said P-channel transistor set.

6. (Previously Presented) The device of claim 5, wherein activation of at least one of said P-channel and said N-channel transistor sets provides a switching on of said capacitive delay upon said input signal to provide a delayed output signal.

7. (Previously Presented) The device of claim 5, wherein de-activation of at least one of said P-channel and said N-channel transistor sets provides a switching off of said capacitive delay upon said input signal to provide an output signal with less delay.

8. (Original) The device of claim 5, further comprising a plurality of N-channel transistor sets and P-channel transistor sets to provide additional delays upon said input signal to provide a delayed output signal.

9. (Previously Presented) The device of claim 4, wherein said output signal comprises said coarse delay and said fine delay.

10. (Original) The device of claim 1, wherein said reference signal is a clock signal.

11. – 24 (Cancelled).

25. (Previously Presented) A system board, comprising:

a first device comprising a memory location for storing data and a delay lock loop to provide an output signal based upon a phase difference between a reference signal and a feedback signal, said delay lock loop comprising a delay circuit for activating a transistive capacitive delay; and

a second device operatively coupled to said first device, said second device to access said data from said first device based upon an operation performed by said delay lock loop.

26. (Original) The system board described in claim 25, wherein said memory location is at least one of an SRAM, a DRAM, a DDR SDRAM, a DDR I device, a DDR II device, a RDRAM, and a FLASH memory.

27. (Original) The system board of claim 25, wherein said system board is a motherboard of a computer system.

28. (Previously Presented) The system board of claim 25, wherein said delay lock loop further comprises:

a coarse delay unit to provide a coarse delay upon at least one of said reference signal and a data output signal;

a fine delay unit to provide a fine tuned delay upon at least one of said reference signal and said data output signal;

a phase detector to detect said phase difference; and

a feedback delay unit operatively coupled to said coarse delay unit, said fine delay unit, and said phase detector, said feedback delay unit to provide a delay upon said output signal to generate said feedback signal.

29. (Previously Presented) The system board of claim 28, wherein said fine delay unit comprises:

a first inverter to invert an input signal;

an N-channel transistor set operatively coupled to said first inverter, said N-channel transistor set comprising a first and a second N-channel transistor, wherein a source terminal of said first N-channel transistor is coupled to a source terminal of said second N-channel transistor and a drain terminal of said first N-channel transistor is coupled to a drain terminal of said second N-channel transistor;

an P-channel transistor set comprising a first and a second P-channel transistor, wherein a source terminal of said first P-channel transistor is coupled to a source terminal of said second P-channel transistor and a drain terminal of said first P-channel transistor is coupled to a drain terminal of said second P-channel transistor; and

a second inverter operatively coupled to said P-channel transistor, said second inverter to provide a complementary control signal for said P-channel transistor set.

30. (Previously Presented) The system board of claim 29, wherein activation of at least one of said P-channel and said N-channel transistor sets provides said switching on of a capacitive delay upon said input signal to provide a delayed output signal.

31. (Previously Presented) The system board of claim 29, wherein de-activation of at least one of said P-channel and said N-channel transistor sets provides said switching off of a capacitive delay upon said input signal to provide an output signal with less delay.

32. (Original) The system board of claim 29, further comprising a plurality of N-channel transistor sets and P-channel transistor sets to provide additional delays upon said input signal to provide a delayed output signal.

33. (Previously Presented) The system board of claim 28, wherein said output signal comprises said coarse delay and said fine delay.

34. (Original) The device of claim 25, wherein said reference signal is a clock signal.

35. (Previously Presented) A memory device, comprising:

delay lock loop to provide an output signal based upon a phase difference between a reference signal and a feedback signal, said delay lock loop comprising a delay circuit activating a transistive capacitive delay.

36. (Original) The memory device of claim 35, wherein said memory device is at least one of a static random access memory (SRAM), a dynamic random access memory (DRAM), a double-data rate SDRAM (DDR SDRAM), a DDR I device, a DDR II device, a Rambus DRAM (RDRAM), and a FLASH memory.

37. (Previously Presented) The memory device of claim 35, wherein said delay lock loop further comprises:

a coarse delay unit to provide a coarse delay upon at least one of said reference signal and a data output signal;

a fine delay unit to provide a fine tuned delay upon at least one of said reference signal and said data output signal;

a phase detector to detect said phase difference; and

a feedback delay unit operatively coupled to said coarse delay unit, said fine delay unit, and said phase detector, said feedback delay unit to provide a delay upon said output signal to generate said feedback signal.

38. (Original) The memory device of claim 37, wherein said fine delay unit comprises at least one delay block, said delay block to provide a delay upon at least one of said reference signal and said data output signal.

39. (Original) The memory device of claim 38, wherein said delay block comprises:

a first inverter to invert an input signal;

an N-channel transistor set comprising a first and a second N-channel transistor, wherein a source terminal of said first N-channel transistor is coupled to a source terminal of said second N-channel transistor and a drain terminal of said first N-channel transistor is coupled to a drain terminal of said second N-channel transistor;

an P-channel transistor set comprising a first and a second P-channel transistor, wherein a source terminal of said first P-channel transistor is coupled to a source terminal of said second P-channel transistor and a drain terminal of said first P-channel transistor is coupled to a drain terminal of said second P-channel transistor; and

a second inverter to provide a complementary control signal for said P-channel transistor set.

40. (Previously Presented) The memory device of claim 39, wherein activation of at least one of said P-channel and said N-channel transistor sets provides a switching on of said capacitive delay upon said input signal to provide a delayed output signal.

41. (Previously Presented) The memory device of claim 39, wherein de-activation of at least one of said P-channel and said N-channel transistor sets provides a switching off of said capacitive delay upon said input signal to provide an output signal with less delay.

42. (Original) The memory device of claim 39, further comprising a plurality of N-channel transistor sets and P-channel transistor sets to provide additional delays upon said input signal to provide a delayed output signal.

43. (Previously Presented) The memory device of claim 37, wherein said output signal comprises said coarse delay and said fine delay.

44. (Original) The device of claim 43, wherein said reference signal is a clock signal.

45. – 49. (Cancelled).